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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,030	11/24/2003	Taketo Heishi	67471-030	5444
Michael E Foga	7590 12/27/2007	003 Taketo Heishi 12/27/2007	EXAMINER	
McDermott Will & Emery			PAN, DANIEL H	
Suite 1200	7590 12/27/2007 E Fogarty nott Will & Emery 1 Street NW		ART UNIT	PAPER NUMBER
Washington, DC 20005-3096			2183	
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			MAIL DATE	DELIVERY MODE
			12/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)				
		HEISHI ET AL.				
Office Action Summary	10/720,030					
Office Action Cummary	Examiner	Art Unit				
The MAILING DATE of this communication and	Daniel Pan	2183				
- The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on 24 Se	eptember 2007.					
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	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4) Claim(s) 40-54 is/are pending in the application.						
4a) Of the above claim(s) <u>1-39</u> is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>40-54</u> is/are rejected.						
7) Claim(s) is/are objected to.						
8) Claim(s) are subject to restriction and/or election requirement.						
Application Papers						
9)☐ The specification is objected to by the Examine	r.					
10)⊠ The drawing(s) filed on 24 November 2003 is/a	re: a)⊠ accepted or b)⊡ obje	ected to by the Examiner.				
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)⊠ All b)□ Some * c)□ None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No. 09/280,777.						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(c)						
Attachment(s) 1) Notice of References Cited (PTO-892)	4) Interview Summ	ary (PTO-413)				
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mai					
3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 11/24/03,11/20/06.	5) Notice of Informa 6) Other:	я і аквік пррівовион				

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Claims 40-54 arte presented for examination. Claims 1-39 have been canceled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 1. Claims 40-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Sato et al. (5,488,710).
- 2. As to claims 40,41, 47,48, Taught a system comprising (see fig.6):
- a) an execution unit for executing up to N number of instructions (4) having a variable bit length in parallel (see parallel variable length in fig.6), the maximum bit length of an instruction that is executed in parallel is M bits (16);
- b) an instruction supplying/issuing unit which fetches an instruction sequence in a unit of a first bit length of code (1 bit units of total 64) and outputs the instruction sequence in a unit of a second bit length of code (16);
- c) a decoding unit which decodes the instruction sequence in a unit of a variable bit length of code which is at least a part of the second bit length of code (16) outputted by the instruction supplying/issuing unit, and outputting a decoding result to the execution unit (see execution unit and decoding unit in col.6, lines 16-54, see also in fig.9c and in col.8, lines 3-52 alternative embodiment for the simultaneous execution of instructions)

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- c) an instruction bus formed between the instruction supplying/issuing unit and the decoding unit, wherein the total bit width of the instruction bus is shorter than 16 * 4 bits (see output of instruction latches [211] and decoders 221 in fig.6).
- 3. As to claims 42,49, examiner holds that instructions had to be in a form of a high-level instruction before being converted or decoded, such as a source code.
- 4. As to claims 43, 50, , the first length was also shorter (1 bit <16 bit).
- 5. As to claims 44,51,53, see fig.9c and in col.8, lines 3-52 alternative embodiment for the simultaneous execution of instructions.
- 6. As to claims 45, 52, also taught instruction boundary (see instruction bit width indication in fig.6).
- 7. As to claim 54, see instruction latches for temporally storing instructions (fig.6 [instruction latch]).
- 8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- a) Chu et al. (4,785,393) is cited for the teaching of conversion of variable bit instruction including the width positions (see col.8, lines 37-68, col.9, lines 1-47);
- b) Sanders et al. (5,006,980) is cited for the specific format of the prefetch of variable length instruction (see col.10, lines 24-64.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172.

The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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